Claims

1. Method of addressing a plurality of microsystems (2) which can be individually addressed by a control circuit (3), the control circuit (3) and each microsystem (2) comprising electromagnetic transmission means (4, 5, 8, 11), each microsystem (2) comprising a counter (14) and having an addressing code, an addressing phase of the microsystems (2) comprising transmission, by the control circuit (3), of successive increment signals (S1, S2, S3), each microsystem (2) monitoring resetting of its counter (14) and, upon receipt of an increment signal (S1), incrementation of the content (Sc) of its counter (14), and each microsystem (2) comparing the content (Sc, C) of its counter (14) and its addressing code, so as to trigger execution of a pre-determined command when the content (Sc) of its counter (14) and its addressing code are identical, method characterized in that, the microsystems (2) forming an array (1) of microsystems (2), each microsystem comprises an identification code (ID), in a read-only memory (15), and the method comprises an initialization phase successively comprising, for each microsystem (2), addressing, by the control circuit (3), of the microsystem (2) by its identification code (ID) and storing of a reduced addressing code (C) supplied by the control circuit (3) in a register (13) of the microsystem (2).

2. Method of addressing according to claim 1, characterized in that the reduced addressing code (C) of a microsystem (2) is a function of its position in the array (1).

3. Method of addressing according to one of the claims 1 and 2, characterized in that the reduced addressing codes (C) of the microsystems (2) correspond to increasing numbers starting from a first microsystem.

4. Method of addressing according to any one of the claims 1 to 3, characterized in that the microsystems (2) are arranged in lines and columns, the reduced addressing code (C) of each microsystem (2) comprising a line number and a column number respectively stored in line and column registers (13) of the microsystem (2), the contents (C) of the line and column registers (13) being respectively compared with the contents (Sc) of the line and column counters (14) of the microsystem.

5. Method of addressing according to claim 4, characterized in that the control circuit (3) successively transmits line increment signals (S1) and column increment signals (S2), the line increment signals (S1) causing the content (Sc) of the line counters (14) to be incremented and the column increment signals (S2) causing the content (Sc) of the column counters (14) to be incremented and the line counters (14) of all the microsystems (2) to be reset.

6. Method of addressing according to claim 5, characterized in that the microsystems (2) are arranged in lines, in columns and according to height, the reduced addressing code (C) comprising an additional number associated to the height, stored in an additional register (13) associated to the height, each microsystem (2) comprising an additional counter (14) associated to the height, the content (C) of the register (13) associated to the height being compared with the content (Sc) of the counter (14) associated to the height.

7. Method of addressing according to claim 6, characterized in that the control circuit (3) transmits height increment signals (S3) causing the additional

counters (14) associated to the height to be incremented and the line and column counters (14) of all the microsystems (2) to be reset.

8. Method of addressing according to any one of the claims 1 to 7, characterized in that a microsystem (2) transmits an acquit signal after the latter has executed its command.

9. Method of addressing according to any one of the claims 1 to 8, characterized in that the control circuit (3) transmits data representative of the type of command to be executed by the microsystems (2) in association with transmission of a reset signal (RAZ).

10. Method of addressing according to any one of the claims 1 to 9, characterized in that the control circuit (3) transmits data representative of the type of command to be executed by the microsystems (2) in association with transmission of an increment signal (S1, S2, S3).